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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	: Atty. Docket No. POU920010166US1
Marvin J. RICH et al.	: Group Art Unit: 2123
Serial No.: 10/038,689	: Examiner: Not Yet Assigned
Confirmation No.: 4133	:
Filed: January 2, 2002	:

For: *VHDL TECHNOLOGY LIBRARY METHOD FOR EFFICIENT CUSTOMIZATION OF CHIP GATE DELAYS*

SUBMISSION OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Box Missing Parts
Washington, D.C. 20231

Sir:

Submitted herewith are 22 sheets of formal drawings containing Figures 1-22 for the above-identified application.

The Commissioner is authorized to charge any fees or credit any overpayment to Deposit Account No. **09-0463.**

Respectfully submitted,

Date: 2/28/02

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